



ocket No.: 57454-011

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Akira YAMAZAKI, et al.

Serial No.: 09/780,477

Group Art Unit: 2816

Filed: February 12, 2001

Examiner: TRA, ANH QUAN

For: MULTI-POWER SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

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☐

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	24	20	4	\$18.00 =	\$72.00
Independent Claims	4	4	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
Total of Above Calculations					\$72.00

☒ Please charge my Deposit Account No. 500417 in the amount of \$72.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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Date: February 7, 2003



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AMENDMENT

Box AF
Commissioner for Patents
Washington, DC 20231

Sir:

Submitted concurrently herewith is a Request for Continued Examination. In response to the Final Rejection dated November 7, 2002, Applicants respectfully submit the following remarks and amendments.

IN THE CLAIMS:

Please amend claims 1, 11, 19 and 20 to read as follows:

1. (TWICE AMENDED) A semiconductor integrated circuit device comprising:
- a first power-on detection circuit responsive to a first power supply voltage for detecting power-on of said first power supply voltage to activate a first power-on detection signal according to a result of detection;
- a second power-on detection circuit responsive to a second power supply voltage for detecting power-on of said second power supply voltage independently of a voltage level of said first power supply voltage, to activate a second power-on detection signal according to a result of